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Dual Gated Silicon Nanowire Field Effect Transistors

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Abstract

Silicon Nanowire field effect transistors (SiNWFETs) are ideal candidates for basic sensing units. We report here on a top down fabrication process in SOI wafers yielding SiNWFETs. We operate the SiNWFETs in a liquid cell and control their operation with two gates: a liquid gate and a back gate. We compare the combined effects of the two gates (dual gating) on the transport characteristics in electrolytes and show that both gates are essential to perform well-defined sensing experiments.

Keywords: Silicon Nanowires, pH sensing, FET, ISFET, Electrolyte Gate, SOI

1. Introduction

In the perspective of directly integrating chemical sensing into electronic devices, Ion Sensitive Field Effect Transistors (ISFETs) have been introduced in the 70-ies [1]. The idea of gating a Field Effect Transistor (FET) was recently transferred to FETs based on carbon nanotube (CNT) [2] and nanowires (NW) [3, 4]. First studies demonstrated the sensitivity of CNTFETs to oxidizing or reducing gases [5], electrolyte gating [6] and were followed by reports describing the detection of toxic gases, pH changes, proteins and DNA with NWFETs [7-9] and CNTFETs [10]. This high interest is driven by the size compatibility between the sensor and the sensed species. The high surface to volume ratio enhances the sensitivity of the sensor [11], allows the detection of low analyte concentrations (down to the fM range) [12] and a fast response time. Such features anticipate the integration of the sensors into large-scale arrays combined with micro-fluidics for the development of highly integrated sensor chips. Arrays of sensors open possibilities to correlate measurements in time and space for identical sensors [13] and permit multiplex measurements in arrays with differently functionalized sensors. The latter approach is important to ensure reliable disease diagnosis, which often requires the identification of multiple molecular markers [14]. While convincing biosensing experiments with both SiNWFETs and CNTFETs have been reported, real-life applications will still require improved control, together with a detailed understanding of the basic sensing mechanisms. For this reason, pH sensing is under careful investigation in SiNWFETs [11, 12] as well as electrochemical aspects of CNTFETs in ionic solutions. Fabrication issues like locating and contacting problems [3,5] can be circumvented by using a top-down approach where silicon nanowire are directly etched into the wafer [12]. We report here on a scalable fabrication process based on a “standard” top-down approach by etching the nanowire structures directly in silicon on insulator (SOI) wafers [12]. This method has unrivalled advantages including well-controlled wire

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properties, no positioning issues and an easy integration with micro-fluidics. The wires show an ambipolar behaviour with good electrons and holes mobilities and a relatively low density of surface traps. The carrier density can be modulated either via an electric field applied via a back-gate as well as by the electrostatic potential of the surrounding liquid and of chemicals adsorbed on the nanowire. Whereas electrolyte-gating has been investigated in standard ISFETs as well as for CNTFETs, we compare the SiNWFET here in complement to a back-gating action. We show that the dual-gate geometry results in a robust experimental approach and we demonstrate pH sensitivity.

2. Silicon Nanowire FETs

SiNWFETs were produced by lithographic means into the device layer of a SOI wafer (Simgui). The SOI wafer is lightly boron doped with a resistivity of 10-20 Ωcm and consists of a 100 nm thick silicon device layer, 150 nm SiO_2 insulating layer (BOX) and a 500 μm thick silicon substrate. The device layer was thinned to 60 nm by thermal oxidation leading to a top SiO_2 layer of about 80 nm. The silicon nanowire structures are typically 1-10 μm long and have typical widths of 100 nm up to 1 μm . The samples are patterned by lithographic means. A lift-off process is used to structure a 60 nm-thick chromium layer working as a mask. The structure is then transferred into the SOI wafer by reactive ion etching and a wet etching process using buffered hydrofluoric acid (BHF) and tetra-methyl-ammonium-hydroxide (TMAH). The contacts are produced in an additional lithography step and thermal deposition of aluminum, followed by annealing at 450° C in vacuum to form ohmic contacts. A typical sample in our experiments consists of seven nanowires. Fig. 1(a) shows a SEM picture of a sample with multiple wires and a closer look on a single wire (inset Fig. 1(a)).

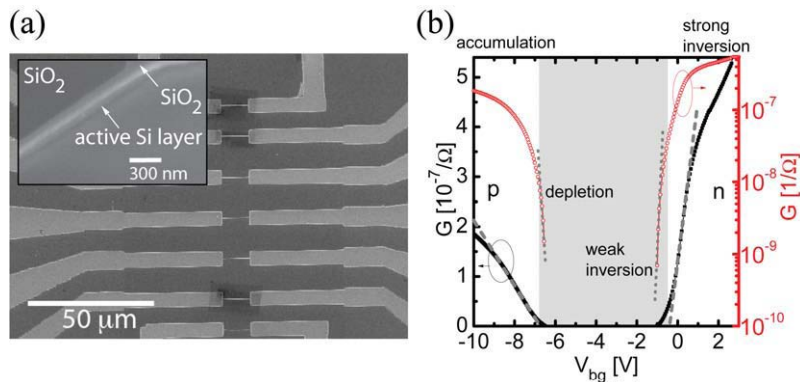


Fig. 1: (a) SEM picture of a typical sample with seven nanowires and leads, all etched into the silicon device layer. The aluminium contacts are not visible. Inset: single nanowire; (b) Typical conductance G vs. back-gate V_{bg} . The graph shows the SiNWFET response in linear (left, black) and logarithmic (right, red) scales.

After wire bonding (Al wire + 1% Si) the devices are characterized by measuring their linear conductance G with lock-in technique at a bias voltage of 10 mV and a frequency of 317 Hz. The response of G to the back-gate voltage V_{bg} for a typical sample is shown in Fig. 1(b). Since Al-Si contacts allow both, hole and electron transport and the leads are semiconducting and low-doped, the silicon nanowire FET shows an ambipolar behaviour. From a fit in the two linear regimes (Fig. 1(b), dashed line), we can estimate the mobilities of the charge carriers. We find mobilities in the range of $\mu = 20..100 \text{ cm}^2/\text{Vs}$ for short wires (about 1 μm length) up to $\mu = 200..1400 \text{ cm}^2/\text{Vs}$ for longer nanowires (10 μm length). Here we used a gate capacitance per unit area of $\sim 10^{-5} \text{ F/m}^2$ as inferred from capacitance spectroscopy. These values are in good agreement with mobilities observed in the device layer of SOI wafers [15].

3. Measurements in Solution and Dual - Gating

To operate the nanowires in electrolyte solutions, we sealed the sample with epoxy (EPOTEK 302-3M) except for a small opening over the wires area, as depicted in Fig. 2(a). This configuration allows us to protect the contacts and expose only the nanowires to the solution. A platinum electrode, which is immersed into the solution, acts as liquid gate. The liquid potential V_{lg} applied to the platinum wire affects only the nanowires exposed to the solution since the contact leads are covered with epoxy. The back-gate potential V_{bg} affects however both the nanowires and contact leads. The geometry depicted in Fig. 2(a) allows combining both types of gating, liquid (top)-gating and back gating, to characterize a device. The result is shown in the dual-gate diagram of Fig. 2(b) where the conductance is represented in a colour-coded contour plot as function of the applied gate voltages V_{bg} and V_{lg} . As electrolyte a 1mM KCl solution in H_2O was used. For positive voltages at both gates, the device is in the n-regime, while for negative voltages it is in the p-regime as depicted by the letters n and p. For $V_{bg} > 0$ and $V_{lg} < 0$ the NW is driven in the p-regime by the electrolyte-gate whereas the leads - insulated from the liquid - are driven in the n-regime by the back-gate. In this case, the device forms a npn-junction. For $V_{bg} < 0$ and $V_{lg} > 0$, we obtain a pnp-junction. In both cases the current is suppressed. The back-gate capacitance C_{bg} is dominated by the 150 nm layer of buried SiO_2 whereas the electrolyte-gate capacitance C_{elg} depends on the double layer capacitance of the electrolyte C_{dl} as well as the native oxide at the side-walls. For 1 mM KCl electrolyte, $C_{elg} > C_{bg}$ and this leads to a more efficient coupling of the electrochemical gate than of the back-gate. This can be seen in the p-regime where the back-gate has very little effect on the conductance for $V_{bg} < -5$ V. Above -5 V, the increasing back-gate potential starts to deplete the leads resulting in a progressive suppression of the conductance. By making use of the back-gate, the device-operating region can be adjusted without any additional need for ion implantation. The dual-gate approach ensures that all electrostatic potentials in the system are well controlled, with the only variable being the surface potential of the NW, which can be modulated by surface charge modifications.

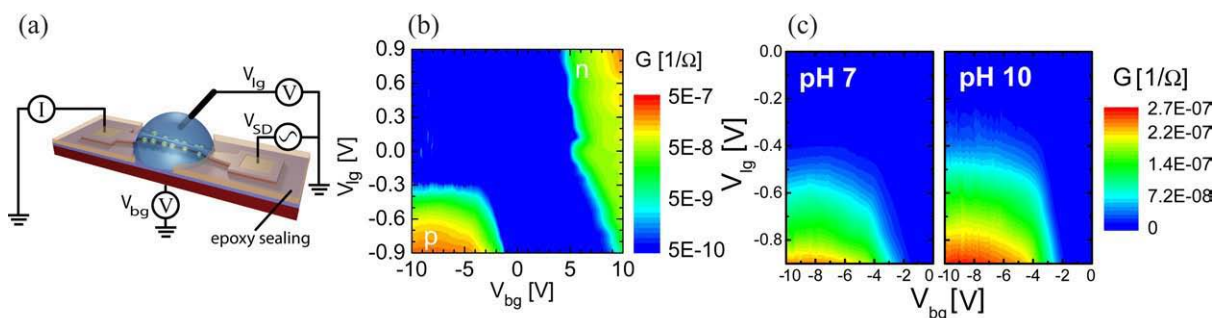


Fig. 2: (a) Sketch of the dual-gate measurement set-up in liquid environment. The electrostatic potential of the liquid is tuned by a platinum electrode (V_{lg}) while applying a back-gate via the Si substrate (V_{bg}). An AC voltage is applied between source and drain (V_{SD} , 10mV, 317Hz). The device is epoxy-sealed except for an opening over the wires area; (b) Dual-gate diagram: Contour plot of conductance (colour-coded) versus back-gate and electrolyte gate in a 1mM KCl solution in H_2O ; (c) Conductance response as function of back-gate and liquid potential for pH 7 and pH 10. Electrolyte: 1mM KCl in H_2O .

The surface charge of the silicon oxide at the NW – liquid interface strongly depends on the pH value of the surrounding electrolyte solution and acts as an additional gating effect [7, 12]. Here we make use of this effect to show how our dual-gated SiNWFETs can be used for the detection of pH changes. The response of the SiNWFETs on the pH value change is shown in Fig. 2(c). The dual-gate diagram in the p-regime is shown for two different pH values of a 1 mM KCl solution in H_2O . For high negative gate voltages the device is in accumulation. The most pronounced effect when comparing measurements at different pH values is the shift in the onset voltage on the V_{lg} axis. At higher pH value the onset of the conductance sets in for less negative V_{lg} .

A qualitative picture of the conductance change can be given if the surface charges of the nanowires are taken into account. A SiO_2 surface bears a large quantity of $-SiOH$ end groups. At basic pH, these groups will deprotonize more easily thereby changing the surface potential of the oxide-electrolyte interface. We can therefore expect that, in

our experiment, a less negative liquid gate voltage needs to be applied at pH 10 in order to drive the nanowire into accumulation. This can qualitatively explain the shift of the conductance onset and increase. Further investigations are underway which will provide a deeper insight into the mechanisms at stake. It is nevertheless clear at this stage that a dual-gate configuration is required to bring the nanowires in the proper conductance regime for pH sensing.

4. Conclusion

We showed that a scalable fabrication process for producing SiNWFETs yields well-defined nanowires with ambipolar properties. We introduced a dual-gated configuration for measurements in liquid. In solution, the effect of pH variation can be observed as a voltage shift of the conductance onset versus electrolyte gate, at an appropriately chosen back-gate voltage. The stronger capacitive coupling of the electrolyte to the nanowire ensures a clearer signal in this configuration than in the more conventional back-gate response. Future developments will consider implementing multiple-wire sensing to combine pH sensitive and reference electrodes directly on-chip.

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